Google scholar system on chip with UART and parity bit check Search Advanced Scholar Search Scholar Preferences

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A portable and fault-tolerant microprocessor based on the SPARC V8 architecture
J Gaisler - 2002 - computer.org
... To avoid the large overhead of spare units, the decision was taken to imple- ment on-**chip** fault-tolerance to both detect and **...** Different types of SEU protection has been used for these three groups, based on their usage in the **system**. **... UARTS** Timers IrqCtrl I/O port AMBA APB **...**
Cited by 94 - Related articles - BL Direct - All 11 versions

[PDF] Concurrent **error** detection schemes for fault-based side-channel ...
R Karri, K Wu, P Mishra, Y Kim - ... CIRCUITS AND **SYSTEMS**, 2002 - Citeseer
... Another attack focused on the **chip**-writing ability of the attacker. **...** 1512 IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND **SYSTEMS**, VOL **...** Signif- icant work has been done to protect the RAM using **parity bit** coding, Hamming coding, etc [2 **...**
Cited by 44 - Related articles - View as HTML - BL Direct - All 14 versions

Error correction **system** for n **bits** using **error** correcting code designed for fewer ...
DG Abdoo, JD Cabello - US Patent 5,490,155, 1996 - Google Patents
... error detection and correction (EDC) circuits are connected to the **system** memory array **...** 4 of 10 IstSDBCHIP NOMENCLATURE 2nd SOB **CHIP** MEMORY DATA ON SOB **CHIP** MEMORY DATA **...** 60 61 122 123 124 125 62 63 126 127 **CHECK BITS CHECK BITS CHECK BITS** 0 0 **...**
Cited by 16 - Related articles - All 2 versions

Backup/restore technique in a microcomputer-based encryption **system**
SB Hamilton, MJ Rosenow - US Patent 5,008,936, 1991 - Google Patents
... 16, 1991 [54] BACKUP/RESTORE TECHNIQUE IN A MICROCOMPUTER-BASED ENCRYPTION **SYSTEM** [75] Inventors: Scott B. Hamilton, Kirkland; Michael J. Rosenow, Issaquah, both of Wash. [73] Assignee: The Exchange **System** Limited Partnership, Bellevue, Wash. **...**
Cited by 13 - Related articles - All 2 versions

Line support processor for data transfer **system**
CW Harris, LO Jevons Jr, RA Loskorn - US Patent 4,494,194, 1985 - Google Patents
... DLI MEMORY 550m M2 MEMORY OUTPUT BUS 1 **PARITY CHECK** 100 ti **PARITY ERROR** (to 600 **...** In asynchronous **systems** the transmission line is in a "Mark" (binary 1) condition in its **...** The "**bit** oriented" protocols (BOPs) may use only two or three specific control characters for **...**
Cited by 19 - Related articles - All 3 versions

Byte-oriented line adapter **system**
RA Loskorn, PD Biehl, RD Catlller - US Patent 4,514,824, 1985 - Google Patents
... I/O bus 10 in order to particularly identify any given selected buffer 45 memory in the **system**. **... Bit** 0 = I **Bit** 1 = 1 USARTCS = **USART Chip** Select-UCS TMRCS = Timer **Chip** Select-TCS **...** remaining **bits** of Register 37 are used for control signals, primarily for the **USART** and Timer. **...**
Cited by 9 - Related articles - All 4 versions

[BOOK] CAN **system** engineering: from theory to practical applications
W Lawrenz - 1997 - books.google.com
... Timing and Signal Amplitude on the CAN Bus Length 186 5.2.1 CAN **Bit** Timing 187 **...** 4 CAN **System** Engineering from Theories to Application 82526 (see par.3.1), which today is **...** by 82527, Philips followed very soon with a so-called BasicCAN implementation - the 82C200 **chip**. **...**

Cited by 179 - Related articles - Library Search - All 4 versions

[PDF] UART IP Core Specification
J Gorban - Architecture - Iontra.org
... This **UART** core is very similar in operation to the standard 16550 **UART chip** with the main exception being **...** In addition, in the 32-**bit** data bus mode a debug interface is present in the **system**. **...** 0. • The Line Control Register is set to communication of 8 **bits** of data, no **parity**, 1 stop **...**
Cited by 5 - Related articles - View as HTML - All 13 versions

A universal smart transducer interface: TTP/A
H Kopetz, M Holzmann, W Elmenreich - Isorc, 2000 - computer.org
... This is important if "on-**chip**" oscillators are in use at the slaves, since these "on-**chip**" oscillators have a bad long-term stability. **...** 5.1 Communication **System ...** Between two consecutive **UART** bytes there is an inter frame gap (IFG) of 1 **bit** cell. **...**
Cited by 52 - Related articles - BL Direct - All 13 versions

[PDF] Serial and UART Tutorial
F Durda - Retrieved November, 2004 - sunet.se
... several patents on the design and they also limited licensing, making it harder for other vendors to provide a **chip** with similar **...** Serial and **UART** Tutorial **...** This over-simplistic criteria means that if a different operating **system** is used, problems could appear due to subtle differences **...**
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